WHAT IS CLAIMED IS:

1. A silicon controlled rectifier structure comprising:

a semiconductor material of a first conductivity type having a top surface and a dopant concentration;

a first well of a second conductivity type formed in the semiconductor material, the first well contacting the top surface of the semiconductor material and having a dopant concentration;

a first semiconductor region of the first conductivity type formed in the first well, the first semiconductor region having a greater dopant concentration than the dopant concentration of the semiconductor material; and

a second semiconductor region of the second conductivity type formed in the first well, the second semiconductor region having a greater dopant concentration than the dopant concentration of the first well.

2. The silicon controlled rectifier structure of claim 1 and further comprising a third semiconductor region of the first conductivity type formed in the semiconductor material, the third semiconductor region contacting the first well and the semiconductor material, being spaced apart from the first and second semiconductor regions, and having a greater dopant concentration than the dopant concentration of the semiconductor material.

3. The silicon controlled rectifier structure of claim 2 and further comprising:

a second well of the second conductivity type formed in the semiconductor material, the second well contacting the top surface of

the semiconductor material, and being spaced apart from the first well; and

a fourth semiconductor region of the first conductivity type formed in the semiconductor material, the fourth semiconductor region contacting the top surface of the semiconductor material, the second well, and the semiconductor material, and having a greater dopant concentration than the dopant concentration of the semiconductor material.

4. The silicon controlled rectifier structure of claim 3 and further comprising a fifth semiconductor region of the first conductivity type formed in the second well, the fifth semiconductor region contacting the top surface of the semiconductor material, being spaced apart from the fourth semiconductor region, and having a greater dopant concentration than the dopant concentration of the semiconductor material.

5. The silicon controlled rectifier structure of claim 4 and further comprising a sixth semiconductor region of the second conductivity type formed in the second well, the sixth semiconductor region contacting the top surface of the semiconductor material, being spaced apart from the fourth semiconductor region, and having a greater dopant concentration than the dopant concentration of the second well.

6. The silicon controlled rectifier structure of claim 5 wherein:

the fifth semiconductor region is spaced apart from a junction between the second well and the semiconductor material; and

the sixth semiconductor region is spaced apart from the junction between the second well and the semiconductor material.

7. The silicon controlled rectifier structure of claim 5 wherein a shortest distance between the second and third semiconductor regions is less than a shortest distance between the fourth and fifth semiconductor regions.

8. The silicon controlled rectifier structure of claim 7 wherein the first and second semiconductor regions are electrically connected together.

9. The silicon controlled rectifier structure of claim 8 wherein the fifth and sixth semiconductor regions are electrically connected together.

10. The silicon controlled rectifier structure of claim 3 wherein the second well surrounds the first well.

11. The silicon controlled rectifier structure of claim 10 wherein the second semiconductor region surrounds the first semiconductor region.

12. The silicon controlled rectifier structure of claim 11 wherein the third semiconductor region surrounds the second semiconductor region.

13. The silicon controlled rectifier structure of claim 12 wherein the fourth semiconductor region surrounds the third semiconductor region.

14. The silicon controlled rectifier structure of claim 13 wherein the fifth semiconductor region surrounds the fourth semiconductor region.

15. The silicon controlled rectifier structure of claim 4 wherein a lateral spacing between the fourth and fifth semiconductor regions is adjusted to set a holding voltage.

16. A method of forming a silicon controlled rectifier structure, the rectifier structure having a semiconductor material of a first conductivity type, the semiconductor material having a top surface, the method comprising the steps of:

forming a first well and a second well of a second conductivity type in the semiconductor material;

forming a plurality of regions of the first conductivity type in the top surface of the semiconductor material so that a first semiconductor region lies in the first well and a second semiconductor region lies the second well; and

forming a plurality of regions of the second conductivity type in the top surface of the semiconductor material so that a third semiconductor region lies in the first well and a fourth semiconductor region lies in the second well.

17. The method of claim 16 wherein the plurality of regions of the first conductivity type include a fifth semiconductor region that

contacts the first well and the semiconductor material, and is spaced apart from the first and the third semiconductor regions.

18. The method of claim 17 wherein the plurality of regions of the first conductivity type include a sixth semiconductor region that contacts the second well and the semiconductor material, and is spaced apart from the second and the fourth semiconductor regions.

19. The method of claim 17 wherein:

the first and third semiconductor regions are spaced apart from a junction between the first well and the semiconductor material; and

the second and fourth semiconductor regions are spaced apart from a junction between the second well and the semiconductor material.

20. The method of claim 17 wherein a shortest distance between the second and third semiconductor regions is less than a shortest distance between the fourth and fifth semiconductor regions.